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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,032	08/18/2003	John C. Pescatore	016295.1401	3223
23640	7590	07/27/2007		
BAKER BOTTS, LLP 910 LOUISIANA HOUSTON, TX 77002-4995			EXAMINER SORRELL, ERON J	
			ART UNIT 2182	PAPER NUMBER
			MAIL DATE 07/27/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/643,032

Applicant(s)

PESCATORE, JOHN C.

Examiner

Eron J. Sorrell

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 21 May 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 12-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 12-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 February 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/21/07 has been entered.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1,5-9, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pekkala et al. (US Pub. No. 2002/0172195 hereinafter "Pekkala") in view of Maezawa et al. (US Patent No. 6,145,024 hereinafter "Maezawa").

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4. Referring to claim 1, Pekkala teaches an information handling system (see figure 1) having a multi-host virtual bridge input-output resource switch (item 106, figure 1), said system comprising:

a plurality of server modules (items 102, figure 1), each of said plurality of server modules having at least one central processing unit (CPU) (item 122, figure 1), memory (item 126, figure 1) and at least one server input-output (I/O) port (item 104, figure 1);

a plurality of input-output (I/O) modules (item 112, figure 1), each of said plurality of input-output modules having a module I/O port adapted for coupling to any one of the at least one server I/O port (see bus connections 116 and 132 connecting I/O modules to the switch); and

at least one input-output (I/O) switch (item 106, figure 1) comprising:

a plurality of input buffers (items 320, figure 3, and item 502, figure 5), wherein a one of the plurality of input buffers is coupled to each of the at least one server I/O port of each of the plurality of server modules and another one of the plurality of input buffers is coupled to the module I/O port of each of the plurality of I/O modules (see figure 3 and paragraph 72 on page 6);

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a plurality of output buffers (items 320, figure 3, and item 504, figure 5), wherein a one of the plurality of output buffers is coupled to each of the at least one server I/O port of each one of the plurality of server modules and another one of the plurality of output buffers is coupled to the module I/O port of each of the plurality of I/O modules (see figure 3 and paragraph 72 on page 6);

a plurality of multiplexers (items 402, figure 4), wherein said plurality of input buffers and said plurality of output buffers are coupled to said plurality of multiplexers (see paragraph 80 on page 8); and

control logic (item 408, figure 4) for controlling said plurality of multiplexers, wherein said plurality of multiplexers determine which ones of said plurality of input buffers are coupled to which ones of said plurality of output buffers (see paragraph 80 on page 8);

the at least one I/O switch (106, figure 1) is coupled to each of the at least one server I/O ports and to each of the module I/O ports, wherein said at least one I/O switch couples selected ones of the at least one server I/O ports to selected ones of the module I/O ports (see paragraph 70 on page 6).

Pekkala fails to teach the I/O switch statically couples selected ports and fails to teach the plurality of server

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modules will boot its operating systems and recognize the statically coupled ones of the I/O ports.

Maezawa teaches, in a system wherein a plurality of servers are connected to a plurality of I/O devices via an I/O switch, statically coupling the server ports to the I/O ports (see lines 46-62 of column 9) and the servers booting the respective operating systems and recognizing the statically coupled ports (see paragraph bridging columns 6 and 7).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Pekkala with the above teachings of Maezawa. One of ordinary skill in the art would have been motivated to make such modification in order to allow data transfer between a plural links and having different data transfer capabilities as suggested by Maezawa (see lines 46-62 of column 9)

5. Referring to claim 5, Pekkala teaches the information handling system further comprises an Ethernet controller in at least one of said plurality of server modules (see paragraph 57 on page 4).

6. Referring to claim 6, Pekkala teaches the at least one server I/O port is a serial port (see paragraph 56 on page 4).

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7. Referring to claim 7, Pekkala teaches the module I/O port is a serial port (see paragraph 53 on page 4).

8. Referring to claim 8, Pekkala teaches the at least one server I/O port is a serial PCI I/O port (see paragraph 59 on page 5).

9. Referring to claim 9, Pekkala teaches the module I/O port is a serial PCI I/O port (see item 206 in figure 2).

10. Referring to claim 12, Pekkala the information handling system further comprises a mapping table coupled to said control logic, said mapping table storing which ones of said plurality of input buffers are coupled to which ones of said plurality of output buffers (see item 412 in figure 4 and paragraphs 106-107 on page 10).

11. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pekkala in view of Maezawa as applied to claim 1 above, and further in view of Applicant's Admitted Prior Art (AAPA).

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12. Referring to claim 2, the combination of Pekkala and Maezawa teaches the system of claim 1 as shown above however the combination fails to teach a bridge for coupling the CPU to the memory and to the at least one server I/O port.

The applicant admits at paragraph 3 of the instant specification, that typically, servers comprise bridges for coupling the CPU, memory, and the I/O port.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Pekkala and Maezawa with the AAPA in order for different proprietary devices to communicate.

13. Claims 3 and 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pekkala in view of Maezawa as applied to claim 1 above and further, in view of Heath et al. (U.S. Patent No. 6,564,274 hereinafter "Heath").

14. Referring to claims 3 and 4, the combination of Pekkala and Maezawa teaches the system of claim 1 as shown above, however the combination fails to teach the information handling system further comprises at least one native input-output (I/O) device in at least one of said plurality of server modules, wherein the at least one native I/O device is an interface selected from the

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group consisting of USB, serial, keyboard, video and mouse interfaces.

Heath teaches, in an analogous system, the above limitations (see paragraphs bridging columns 5 and 6).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Pekkala and Maeawa with the above teachings of Heath in order to give a user access to the server using common peripheral devices (i.e. keyboard, mouse, and monitor).

15. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pekkala in view of Maezawa as applied to claim 1, above and further in view of McMillen et al. (U.S. Patent No. 5,872,904 hereinafter "McMillen").

16. Referring to claims 13 and 14, the combination of Pekkala and Maezawa teaches the system of claim 12 above, however the combination fails to teach the information handling system further comprising initialization logic for initializing said control logic and said mapping table, wherein said initialization logic is external from said at least one I/O switch.

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McMillen teaches, in an analogous system, the above limitations (see lines 10-15 of column 46).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Pekkala and Maezawa with the above teachings of McMillen in order to provide default values for a fully configured network to as suggested by McMillen (see lines 10-15 of column 46).

17. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pekkala in view Maezawa and further in view of McMillen as applied to claims 13 and 14 above, and further in view of Oehler et al. (U.S. Pub No. 2003/0037224 hereinafter "Oehler").

18. Referring to claims 15 and 16, the combination of Pekkala, Maezawa, and McMillen teaches the system of claims 13 and 14 as shown above, however the combination fails to teach the initialization logic is coupled to said control logic with a low pin count interface, wherein the low pin count interface is selected from the group consisting of I2C or JTAG.

Oehler teaches, in an analogous system, the above limitation (see paragraph 39 on page 4).

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It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Pekkala, Maezawa, and McMillen with the above teachings of Oehler in order to allow for both static and dynamic configuring as suggested by McMillen (see paragraph 39 on page 4).

19. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pekkala in view of Maezawa as applied to claim 1 above, and further in view of Lawrence (U.S. Patent No. 6,826,196).

20. Referring to claim 17, the combination of Pekkala and Maezawa teaches the system of claim 1, as shown above, however the combination fails to teach the at least one I/O switch is accessed through a user interface.

Lawrence teaches, in an analogous system, the above limitation (see 54-65 of column 1).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Pekkala and Maezawa with the above teachings of Lawrence in order to allow the user to access and control the switch as suggested by Lawrence (see 54-65 of column 1).

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***Response to Arguments***

21. Applicant's arguments with respect to claim 1 has been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J. Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EJS

7/16/2007

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